UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,501	06/19/2006	Kazuhiro Fujikawa	12967-007US1 905350-02	3685

26211 7590 01/22/2010

FISH & RICHARDSON P.C.
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
YUSHINA, GALINA G	
ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
01/22/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/583,501	FUJIKAWA ET AL.	
	Examiner	Art Unit	
	GALINA YUSHINA	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's response to the Office Non-Final Action filed on 10/26/09 is acknowledged.

2. Applicant submitted new drawings (Fig. 6, and Fig. 7), amended Claims 1, 4, and 5, and added new Claims 10-17.

3. Claims 1-17 are examined on merits herein.

Claim Objection

4. **Claim 5** is objected to. The claim recites "another buffer layer on the first conductivity type". Examiner suggests ""another buffer layer of the first conductivity type".

Claim Rejections - 35 USC § 112

5. **The following is a quotation of the second paragraph of 35 U.S.C. 112**:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph**, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. **In re Claim 1**: The claim recites "a buffer layer of either a first conductivity type or semi-conductive type" in line 3. This is unclear since it infers that "a first conductivity type" is not a semiconductor.

Appropriate correction is required.

For this Office Action, in accordance with page 10, lines 17-23 of the specification, Examiner interpreted the claim such as a buffer layer is either a first conductivity semiconductor layer, or a second conductivity semiconductor layer, or an undoped semiconductor.

8. **In re Claim 1**: The claim recites "a first conductivity type carrier concentration in said buffer layer is lower than a first conductivity type carrier concentration in said first conductivity type semiconductor layer" in lines 7-8. This is unclear since it infers that the entire buffer layer has a first conductivity type carrier concentration lower than a first conductivity type semiconductor layer. However, the buffer layer contacts a second conductivity doped region, as cited in line 5 of the claim, and the buffer layer also contacts a first conductivity semiconductor region; both regions in accordance with the disclosure (page 10 and Fig. 1) have a high carrier concentration. Due to inherently required post-doping annealing process, inter-diffusions regions exist at/near the interface of any two differently doped regions, and, correspondingly, only "at least a portion" of the buffer layer has a carrier concentration lower than "at least a portion" of the first semiconductor region.

Appropriate correction is required.

For this Office Action, Examiner interpreted the claim such that "at least a portion of the buffer region has a carrier concentration lower than at least a portion of the carrier concentration of the first semiconductor region.

9. **In re Claims 10**: The claim recites "a second conductivity type carrier concentration in the buffer layer is lower than a first conductivity type carrier concentration" in lines 7-8.

This is unclear since it infers that the entire buffer layer has a second conductivity type carrier concentration lower than a carrier concentration of the first conductivity type semiconductor layer. However, the buffer layer contacts a second conductivity doped region, as cited in lines 5-6 of the claim; this "second conductivity doped region" in accordance with the disclosure (page 10 and Fig. 1) has a high carrier concentration. Due to inherently required post-doping annealing process, inter-diffusions regions exist at/near the interface of any two differently doped regions, and, correspondingly, only "at least a portion" of the buffer layer has a carrier concentration lower than "at least a portion" of the carrier concentration of the first semiconductor region.

Appropriate correction is required.

For this Office Action, Examiner interpreted the claim such that "at least a portion of the buffer region has a carrier concentration lower than at least a portion of the carrier concentration of the first semiconductor region.

Claim Rejections - 35 USC § 102

10. **The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102** that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. As far as the claim is understood, **Claim 1 is rejected under 35 U.S.C. 102(b)** as being anticipated by Nishizawa (US 4,364,072).

12. **In re Claim 1**, Nishizawa teaches a junction field-effect transistor comprising (Fig. 10b):

- a first conductivity type semiconductor layer (13, n-type, column 17, lines 56-60) having a channel region;
- a buffer layer (19, column 17, line 54) of a first conductivity type, formed on said channel region in the first conductivity type semiconductor layer (13); and
- a second conductivity type doped region (14, column 18, line 3) formed to reach the buffer layer (19), and in the first conductivity type semiconductor layer (13) on said buffer layer, wherein
- a first conductivity type carrier concentration in said buffer layer (19, its carrier concentration is designated as n--, column 18, line 54) is lower than a first conductivity type carrier concentration in said first conductivity type semiconductor layer (13, its carrier concentration is designated as n-, column 17, lines 59-60).

13. As far as the claim is understood, **Claim 10 is rejected under 35 U.S.C. 102(b)** as being anticipated by Beasom (US 4,873,564).

14. **In re Claim 10**, Beasom teaches a junction field-effect transistor comprising (Fig. 3 and Fig. 5, column 5, lines 3-6):

- a first conductivity type semiconductor layer (15, n-type, column 5, lines 14-16) having a channel region (26, column 6, line 16),
- a buffer layer (24, column 5, lines 12-13) of a second conductivity type (p-type) formed on the channel region in the first conductivity type semiconductor layer (15), and
- a second conductivity type doped region (25, column 5, lines 12-13) formed to reach the buffer layer (24), and in the first conductivity type semiconductor layer (25) on the buffer layer (24), wherein (Fig. 5):
- a second conductivity type carrier concentration in at least a portion of the buffer layer (24, at the depth of 17-19 microns) is lower than at least a portion of the first conductivity type carrier concentration in the first conductivity type semiconductor layer (15/26, at the depth of 25-27 microns, column 6, line 16).

Claim Rejections - 35 USC § 103

15. **The following is a quotation of 35 U.S.C. 103(a)** which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. As far as the claims are understood, **Claims 1-8 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Zhao (US 6,841,812) in view of Nishizawa.

17. **In re Claim 1**, Zhao teaches a junction field-effect transistor comprising (Fig. 5C):

- a first conductivity type (n-type) semiconductor layer (40, column 5, line 7) having a channel region, and
- a second conductivity type doped region (60, p-type, column 5, lines 19-20) formed in the first conductivity type semiconductor layer (40).

Zhao fails to teach:

- a buffer layer of either a first conductivity type or semi-conductive type, formed on said channel region in the first conductivity type semiconductor layer;
- a second conductivity type semiconductor layer is reaching a buffer layer,
- a first conductivity type carrier concentration in said buffer layer is lower than a first conductivity type carrier concentration in said first conductivity type semiconductor layer.

Nishizawa teaches (Fig. 10B):

- a buffer layer (19, column 17, line 54) of the first conductivity type formed on said channel region in the first conductivity type semiconductor layer (13, n-type, column 17, lines 56-60);
- a second conductivity type semiconductor layer (14, column 18, line 3) reaching the buffer layer (19), wherein
- a first conductivity type carrier concentration in said buffer layer (19, the carrier concentration is designated as n--,column 18, line 54) is lower than a first conductivity type carrier concentration in said first conductivity type semiconductor layer (13, the carrier concentration is designated as n-, column 17, lines 59-60).

Zhao and Nishizawa are analogous arts because they both are directed towards vertical junction field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Zhao in view of Nishizawa because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to modify Zhao device by adding a buffer layer of the first conductivity type reached by the second conductivity type semiconductor layer where a carrier concentration in at least a portion of the buffer layer is lower than at least a portion of the carrier concentration of the first semiconductor layer (per Nishizawa) in order to improve the quality of the device by reducing its ON resistance and power dissipation (Nishizawa, column 18, lines 15-18).

18. **In re Claim 2**, Zhao, as modified by Nishizawa, teaches the junction field effect transistor according to Claim 1 as cited above, including, per Nishizawa (Fig. 10B) the first conductivity type semiconductor layer (13, column 18, line 7) having a higher carrier concentration than the concentration of the buffer layer (19, column 18, lines 7-9).

Zhao/Nishizawa fails to explicitly teach that said first conductivity type carrier concentration in said buffer layer is not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer. However, Nishizawa, teaching different carrier concentrations in different layers shows that in his device concentrations could differ from 8 times to more than 40 times (column 8, lines 49-52, column 14, lines 67-68). One of ordinary skill in the art must balance many known factors when designing and optimizing a device. As such, varying concentrations in the buffer layer and in the first conductivity type semiconductor layer would not be cause for undue experimentation. *In re Aller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955), see MPEP 2144.05: "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the carrier concentrations in the buffer layer and in the first conductivity type semiconductor layer in order to improve the quality of the device by reducing its ON resistance and power dissipation (Nishizawa, column 18, lines 15-18).

19. **In re Claim 3**, Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 1 as cited above.

Zhao further teaches (Fig. 5C) that said first conductivity type semiconductor layer (40, column 5, line 7) is composed of silicon carbide (due to forming the layer by epitaxial growth from SiC layers and forming the entire transistor from a SiC, (column 4, lines 50-55 and column 5, lines 59-67).

20. **In re Claim 4**, Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 1 as cited above.

Zhao further teaches (Fig. 5C) another second conductivity type doped region (30, column 5, lines 1-2) formed under said channel region (40, column 5, line 7).

21. **In re Claim 5**, Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 1 as cited above.

Zhao teaches (Fig. 5C):

- the channel region (40, column 5, line 7);
- another second conductivity type doped region (50, column 5, lines 17-19) formed to reach a second conductivity type doped region (30, column 5, lines 1-2) formed under said channel region (40) in another first type conductivity semiconductor layer (20, column 4, line 66).

Zhao fails to teach:

- another buffer layer of the first conductivity type formed under the channel region,
- a first conductivity type carrier concentration in said other buffer layer is lower than the first conductivity type carrier concentration in said first conductivity type semiconductor layer.

Nishizawa teaches (Fig. 10A):

- a first conductivity semiconductor layer (13, column 17, lines 55-56)
- a buffer layer (19, column 17, line 47) of the first conductivity type on the border of the channel and under the channel region (under a layer 14, column 11, lines 60-61),
- a first conductivity type carrier concentration in said other buffer layer (19) is lower than the first conductivity type carrier concentration in the first conductivity type semiconductor layer (13, column 18, lines 7-10).

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to modify Zhao/Nishizawa by creating another buffer region under the channel region (and above the Zhao' region 30 which is formed under the channel region 40), wherein the other buffer layer has a lower carrier concentration than the first conductivity type semiconductor layer in order to improve the device parameters, such as to widen the effective channel width (Nishizawa, column 17, lines 49-51) and to increasing the maximum permissible current (Nishizawa, column 4, lines 56-58).

Note that in the Zhao/Nishizawa structure featuring another buffer layer formed on the Zhao second conductivity layer (Zhao, Fig. 5C, 30), a second conductivity layer (Zhao, Fig. 5C, 50) would reach the second buffer layer since a second conductivity layer is formed above a second conductivity layer (Zhao, Fig. 5C, 30).

22. **In re Claim 6**, Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 5 as cited above, including another buffer layer (Nishizawa, Fig. 10A, 19, column 19, line 8) and the first conductivity layer (Nishizawa,

Fig. 10A, 13, column 18, line 7), where another buffer layer (19) has a lower concentration than a first conductivity semiconductor layer (13), (Nishizawa, column 18, lines 6-10).

Zhao/Nishizawa fails to teach that first conductivity type carrier concentration in said another buffer layer is not more than one tenth of said first conductivity type carrier concentration in said first conductivity type semiconductor layer. However, Nishizawa, teaching different carrier concentrations in different layers shows that concentrations could differ from 8 times to more than 40 times (column 8, lines 49-52, column 14, lines 67-68). One of ordinary skill in the art must balance many known factors when designing and optimizing a device. As such, varying concentrations in another buffer layer and in the first conductivity type semiconductor layer would not be cause for undue experimentation. *In re Aller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955), see MPEP 2144.05: "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the carrier concentrations in another buffer layer in order in order to improve the device parameters, such as to widen the effective channel width (Nishizawa, column 17, lines 49-51) and to increasing the maximum permissible current (Nishizawa, column 4, lines 56-58).

23. **In re Claim 7**, Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 1 as cited above.

Zhao further teaches (Fig. 5C) a semiconductor substrate (10, column 4, line 63) composed of n-type silicon carbide, wherein said first conductivity type semiconductor layer (20, column 4, line 66) is formed on one main surface of said semiconductor substrate (10).

24. **In re Claim 8**, Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 7 as cited above.

Zhao teaches a device (Fig. 5C), further comprising:

- a gate electrode (61, column 7, lines 52-53) formed on the surface of said second conductivity type doped region (60, column 5, lines 19-20),
- a source electrode (71, column 8, line 11), formed on the surface of said first conductivity type semiconductor layer (70, 40, column 6, line 16, column 5, line 64) and
- a drain electrode (Fig. 4, 11, column 5, lines 8-10) formed on another main surface of said semiconductor substrate (10, column 4, line 63).

25. As far as the claim is understood, **Claim 9 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Zhao in view of Nishizawa and further in view of Sakamoto et al. (US 6,555,850).

26. **In re Claim 9,** Zhao, as modified by Nishizawa, teaches the junction field-effect transistor according to Claim 7 as cited above, including a gate electrode formed on the surface of said second conductivity type doped region, and a source electrode formed on the surface of said first conductivity type semiconductor layer as shown for Claim 8.

However, both Zhao and Nishizawa teach a vertical type JFET, and they fail to teach a drain electrode is formed on the same surface of the first conductivity semiconductor layer as a source electrode.

Sakamoto teaches (Fig. 5) a lateral JFET, where a drain electrode (13, column 6, line 4) is formed on the same surface of the first conductivity semiconductor layer (2, 6, 7, column 8, Table) as the source electrode (12, column 6, line 4).

Zhao/Nishizawa and Sakamoto are analogues arts because they both are directed towards field effect transistors, and one of ordinary skill in the art would have had a reasonable expectation of success to modify Zhao/Nishizawa in view of Sakamoto because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time of the invention to use the Zhao/Nishizawa device structure with a buffer layer for a lateral transistor (per Sakamoto) in order to improve parameters of lateral transistors and to increase the field of transistors applications.

27. As far as the claims are understood, **Claims 10-12 and 15-16 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Zhao in view of Beasom.

28. **In re Claim 10**, Zhao teaches a junction field-effect transistor comprising (Fig. 5C):

- a first conductivity type semiconductor layer (40, n-type, column 5, line 7) having a channel region, and

- a second conductivity type doped region (60, p-type, column 5, lines 19-20) in the first conductivity type semiconductor layer (40).

Zhao fails to teach:

- a buffer layer of a second conductivity type formed on the channel region in the first conductivity type semiconductor layer,
- a second conductivity region formed to reach the buffer layer,
- a second conductivity type carrier concentration in the buffer layer is lower than a first conductivity type carrier concentration in the first conductivity type semiconductor layer.

Beasom teaches (Fig. 3 and Fig. 5):

- a buffer layer of a second conductivity type (24, p-, column 5, line 13) formed on the channel region (15 under layer 24, column 5, lines 14-17, or 26, column 6, line 16) in the first conductivity type semiconductor layer (15),
- a second conductivity region (25, p+, column 5, line 13) formed to reach the buffer layer (24),
- a second conductivity type carrier concentration in at least a portion of the buffer layer (24, at the depth of 17-19 microns) is lower than at least a portion of the first conductivity type carrier concentration in the first conductivity type semiconductor layer (15/26, at the depth of 25-27 microns, column 6, line 16).

Zhao and Beasom are analogues arts because they both are directed towards field effect transistors, and one of ordinary skill in the art would have had a reasonable

expectation of success to modify Zhao in view of Beasom because they are from the same field of endeavor.

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to modify Zhao device by providing it with a buffer layer on the channel region, contacting the second conductivity type semiconductor layer and having a lower carrier concentration than a carrier concentration of a first conductivity type semiconductor layer in order to improve the device parameters, such as to reduce the ON resistance of the JFET (Beasom, Abstract).

29. **In re Claim 11**, Zhao, as modified by Beasom, teaches the junction field-effect transistor according to Claim 10 as cited above.

Zhao further teaches (Fig. 5C) that said first conductivity type semiconductor layer (40, column 5, line 7) is composed of silicon carbide (due to forming the layer by epitaxial growth from SiC layers and forming the entire transistor from a SiC, column 4, lines 50-55, and column 5, lines 59-67).

30. **In re Claim 12,** Zhao, as modified by Beasom, teaches the junction field-effect transistor according to Claim 10 as cited above.

Zhao further teaches (Fig. 5C) another second conductivity type doped region (30, column 5, lines 1-2) formed under said channel region (40, column 5, line 7).

31. **In re Claim 15**, Zhao, as modified by Beasom, teaches the junction field-effect transistor according to Claim 10 as cited above.

Zhao teaches a device further comprising (Fig. 5C):

- a semiconductor substrate (10, column 4, lines 62-64) composed of n-type silicon carbide, wherein
- the first conductivity type semiconductor layer (40, column 5, line 7) is formed on one main surface of the semiconductor substrate (10).

32. **In re Claim 16**, Zhao, as modified by Beasom, teaches the junction field-effect transistor according to Claim 15 as cited above.

Zhao further teaches (Fig. 5C):

- a gate electrode (61, column 5, lines 21-23) on the surface of the second conductivity type doped region (60, column 5, line 50),
- a source electrode (71, column 5 line 26) on the top surface of the first conductivity type semiconductor layer (40, column 5, line 7), and
- a drain electrode (Fig. 4, 11, column 5, lines 9-10) on another main surface (a bottom surface) of the semiconductor substrate (10, column 4, lines 62-64).

33. As far as the claims are understood, **Claims 13-14 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Zhao in view of Beasom and further in view of Nishizawa.

34. **In re Claim 13**, Zhao, as modified by Beasom, teaches the junction field-effect transistor according to Claim 10 as cited above.

Zhao teaches the device further comprising (Fig. 5C):

- the channel region (40, column 5, line 7), and

- a third second conductivity type region (30, column 5, lines 1-2) formed under the channel layer (30),
- another second conductivity type doped region (50, column 5, lines 17-18) that reaches the a third second conductivity type region (30) and is in another first conductivity type semiconductor layer (20, column 4, line 66).

Zhao/Beasom fails to teach:

- another buffer layer of the first conductivity type under the channel region,
- another second conductivity type doped region reaches the other buffer layer, wherein
- a first conductivity type carrier concentration in the other buffer layer is lower than a first conductivity type carrier concentration in the first conductivity type semiconductor layer.

Nishizawa teaches (Fig. 10A):

- a first conductivity semiconductor layer (13, column 17, lines 55-56)
- a buffer layer (19, column 17, line 47) of the first conductivity type partially formed directly under the channel region (under a layer 14, column 11, lines 60-61),
- a first conductivity type carrier concentration in said other buffer layer (19) is lower than the first conductivity type carrier concentration in the first conductivity type semiconductor layer (13, column 18, lines 7-10).

It would have been obvious for one of ordinary skill in the art at the time when the invention was made to modify Zhao/Beasom device by creating another buffer region

directly under the channel region (per Nishizawa) and above the Zhao' region 30 wherein the other buffer layer has a lower carrier concentration than the first conductivity type semiconductor layer in order to improve the device parameters, such as to widen the effective channel width (Nishizawa, column 17, lines 49-51) and to increasing the maximum permissible current (Nishizawa, column 4, lines 56-58).

Note that in the Zhao/Beasom/Nishizawa structure featuring another buffer layer formed on the Zhao second conductivity layer (Zhao, Fig. 5C, 30), a second conductivity layer (Zhao, Fig. 5C, 50) would reach the second buffer layer as well since a second conductivity layer reaches a lower located second conductivity layer (Zhao, Fig. 5C, 30).

35. **In re Claim 14**, Zhao, as modified by Beasom and Nishizawa, teaches the junction field-effect transistor according to Claim 13 as cited above, including another buffer layer (Nishizawa, Fig. 10A, 19, column 19, line 8) and the first conductivity semiconductor layer (Nishizawa, Fig. 10A, 13, column 18, line 7), where another buffer layer (19) has a lower concentration than the first conductivity semiconductor layer (13), (Nishizawa, column 18, lines 6-10).

Zhao/Beasom/Nishizawa fails to teach that first conductivity type carrier concentration the other buffer layer is not more than one tenth of the first conductivity type carrier concentration in the first conductivity type semiconductor layer. However, Nishizawa, teaching different carrier concentrations in different layers shows that concentrations could differ from 8 times to more than 40 times (column 8, lines 49-52, column 14, lines 67-68). One of ordinary skill in the art must balance many known factors when designing and optimizing a device. As such, varying concentrations in

another buffer layer and in the first conductivity type semiconductor layer would not be cause for undue experimentation. *In re Aller,* 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955), see MPEP 2144.05: "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the carrier concentrations in another buffer layer (such as making it in the other buffer layer is not more than one tenth of the first conductivity type carrier concentration in the first conductivity semiconductor layer) in order to improve the device parameters, such as to widen the effective channel width (Nishizawa, column 17, lines 49-51) and to increasing the maximum permissible current (Nishizawa, column 4, lines 56-58).

36. As far as the claim is understood, **Claim 17 is rejected under 35 U.S.C. 103(a)** as being unpatentable over Zhao in view of Beasom and further in view of Sakamoto.

37. **In re Claim 17**, Zhao, as modified by Beasom, teaches the junction field-effect transistor according to Claim 15 as cited above.

Zhao teaches the device further comprising (Fig. 5C):

- a gate electrode (61, column 5, lines 21-23) on the surface of the second conductivity type doped region (60, column 5, lines 19-20),
- a source electrode (71, column 5 line 26) on the surface of the first conductivity type semiconductor layer (40, column 5, line 7), and
- a drain electrode (Fig. 4, 11, column 5, lines 9-10).

Zhao fails to teach that a drain electrode is formed on the same surface of the first conductivity semiconductor layer where a source electrode is formed. Beasom, though teaching a lateral transistor (Fig. 3) fails to point out that that a source electrode and the gate electrode are formed on the same surface of the first conductivity semiconductor layer.

Sakamoto teaches (Fig. 5) a lateral JFET, where a drain electrode (13, column 6, line 4) is formed on the same surface of the first conductivity semiconductor layer (2, 6, 7, column 8, Table) as the source electrode (12, column 6, line 4).

It would have been obvious for one of ordinary skill in the art at the time of the invention to use the Zhao/Beasom device structure for a lateral transistor (per Sakamoto) in order to improve parameters of lateral transistors and to increase the field of transistors applications.

The Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Ueno (US 6,303,947) teaches a vertical SiC JFET with the first type conductivity drift layer, and a few second-type conductivity layers, one of which is formed above the channel, another is formed under the channel, and a third layer reaches the layer formed under the channel layer.
- Cheek et al. (US 6,566,696) teaches a lateral transistor having a buffer layer of the same conductivity as the channel layer and formed on the channel layer.

- Kumar et al. (US 2002/0167011) teaches a SiC vertical transistor with a second conductivity layer formed under the channel layer, and a second conductivity region formed to reach this second conductivity layer.
- Disney (US 6,468,847) teaches a second conductivity buffer layer formed on the first conductivity channel layer.
- Fujikawa et al. (US 2006/0113574, the English version of the WO 2004112150, published in December, 2004) and Harada et al. (US 2002/0190258) teach a junction field effect transistor with a buffer layer and a SiC substrate.
- Kato et al. (US 2002/0003245) teaches a lateral transistor comprising two buffer layers.
- Nonaka et al. (US 4,807,011) and Kumar et al. (US 2002/0139992) teach a second conductivity type semiconductor layer formed under the channel layer.
- Kuwata (US 5,331,410) teaches a vertical transistor having two undoped buffers layers above the channel and one undoped buffer layer under the channel.
- Beasom (US 4,961,027) teaches that impurity concentration in the channel defines threshold voltage.

Response to Arguments

38. Applicant's arguments with respect to Claim 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

39. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GALINA YUSHINA whose telephone number is (571)-270-7440. The examiner can normally be reached on Monday through Friday, 7:30 to 5, 5/4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Galina Yushina/
Patent Examiner, Art Unit 2811
01/15/2010

/Lynne A. Gurley/
Supervisory Patent Examiner, Art Unit 2811